IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) ~~Phase~~ A phase detector for a phase-locked loop for digital input signals in which the digital summed value for a particular number of bits is equivalent to Zero, said phase detector comprising ~~having~~ a sampled and digitized data signal being supplied to ~~it~~ said phase detector, ~~having~~ a delay stage for delaying the data signal by one or more sampling clock periods, ~~having~~ a subtraction stage~~,~~ to which the undelayed and the delayed data signal are supplied to produce a differential value, and ~~comprising~~ a filter or control stage to which the output of the subtraction stage ~~are~~ is supplied at ~~whose~~ the output of the filter or control stage which the phase error can be tapped off, ~~wherein~~ characterized in that a processing stage is provided, located between the subtraction stage and the filter or control stage, which assigns one of ~~a~~ the plurality of possible output values, to the respective differential value, wherein ~~the~~ a full differential value range is subdivided in a number of sub-ranges corresponding to ~~the~~ a plurality of possible output values, so that all of the said differential values in one of the sub-ranges will get the same output value assigned.

2. (Currently Amended) ~~Phase~~ The phase detector ~~for a phase-locked loop, said phase detector having a sampled and digitized data signal supplied to it, having a delay stage (52) for delaying the data signal by one or more sampling clock periods, characterized in that a comparison stage is provided which compares a delayed sample with an undelayed sample and assigns one defined value from a plurality of possible values, particularly +1, -1, 0, to the respective comparison result, and in that the assigned values are supplied to a filter/control stage (60), particularly a PI controller, at whose output the phase error can be tapped off~~ according to Claim 1, wherein the subtraction stage is integrated in a comparison stage which compares the delayed sample with said undelayed sample and assigns said one of a plurality of output values to the respective differential value.

3. (Currently Amended) ~~Phase~~ The phase detector according to Claim 1, wherein said filter or control stage is a ~~PI~~ Proportional Integral (PI) controller.

4. (Currently Amended) ~~Phase~~ The phase detector according to Claim 1, in which the delayed digital sample is deducted from the undelayed digital sample in the subtraction stage ~~in each case~~.

5. (Currently Amended) ~~Phase~~ The phase detector according to Claim 1, in which a rectifier for signal conditioning is provided which has the sampled and digitized data signal supplied to it, the data signal being a ternary data signal, in particular.

6. (Currently Amended) ~~Phase~~ The phase detector according to Claim 5, in which the sampled and digitized ternary data signal is supplied, before rectification, to a separating stage in which the data signal is separated into a positive and a negative path.

7. (Currently Amended) ~~Phase~~ The phase detector according to Claim 6, in which separate delay, subtraction and processing stages or delay and comparison stages are provided for each path, and in which an addition stage is provided in which the assigned output values from ~~the~~ one of either processing or comparison stages are added and, combined in this way, are passed on to the filter or control stage.

8. (Currently Amended) ~~Phase~~ The phase detector according to Claim 7, in which, in addition to the separate delay, subtraction and processing stages or delay and comparison stages for the positive and the negative path, there are also separate delay, subtraction and processing stages or delay and comparison stages for a further path, in which the complete data signal~~, including the positive and the negative path,~~ is processed, the output values assigned by the processing stages or comparison stages likewise being supplied to the addition stage.

9. (Currently Amended) ~~Use of the~~ The phase detector according to Claim 1, wherein the phase detector is integrated in a phase-locked loop circuit ~~to recover~~ for recovering the data clock signal for a digital signal.

10. (Currently Amended) ~~Use~~ The phase detector according to Claim ~~8~~ 9, wherein the ~~sampling clock signal for sampling the data signal~~ data signal delayed by one or more sampling clock periods ~~corresponding~~ corresponds to the data clock signal in the data signal.